

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS144C – APRIL 1985 – REVISED MAY 2010

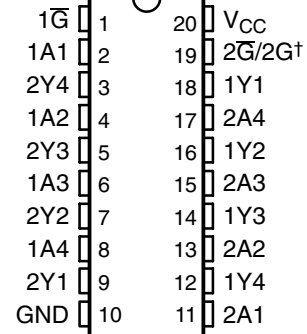
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control (\overline{G}) inputs, and complementary output-control (G and \overline{G}) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω .

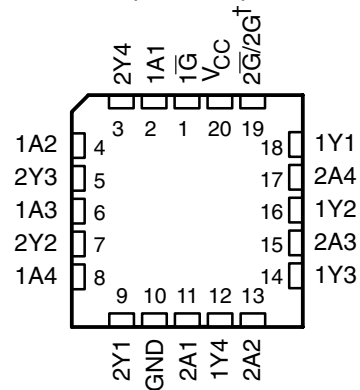
SN54LS', SN54S' ... J OR W PACKAGE
SN74LS240, SN74LS244 ... DB, DW, N, OR NS PACKAGE
SN74LS241 ... DW, N, OR NS PACKAGE
SN74S' ... DW OR N PACKAGE

(TOP VIEW)



† 2G for 'LS241 and 'S241 or $2\overline{G}$ for all other drivers.

SN54LS', SN54S' ... FK PACKAGE
(TOP VIEW)



† 2G for 'LS241 and 'S241 or $2\overline{G}$ for all other drivers.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS240N	SN74LS240N
			SN74LS241N	SN74LS241N
			SN74LS244N	SN74LS244N
			SN74S240N	SN74S240N
			SN74S241N	SN74S241N
			SN74S244N	SN74S244N
	SOIC – DW	Tube	SN74LS240DW	LS240
		Tape and reel	SN74LS240DWR	
		Tube	SN74LS241DW	LS241
		Tape and reel	SN74LS241DWR	
		Tube	SN74LS244DW	LS244
		Tape and reel	SN74LS244DWR	
		Tube	SN74S240DW	S240
		Tape and reel	SN74S240DWR	
		Tube	SN74S241DW	S241
		Tape and reel	SN74S241DWR	
		Tube	SN74S244DW	S244
		Tape and reel	SN74S244DWR	
	SOP – NS	Tape and reel	SN74LS240NSR	74LS240
			SN74LS241NSR	74LS241
			SN74LS244NSR	74LS244
	SSOP – DB	Tape and reel	SN74LS240DBR	LS240
			SN74LS244DBR	LS244

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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ORDERING INFORMATION† (CONTINUED)

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – J	Tube	SN54LS240J	SN54LS240J
			SNJ54LS240J	SNJ54LS240J
			SN54LS241J	SN54LS241J
			SNJ54LS241J	SNJ54LS241J
			SN54LS244J	SN54LS244J
			SNJ54LS244J	SNJ54LS244J
			SN54S240J	SN54S240J
			SNJ54S240J	SNJ54S240J
			SN54S241J	SN54S241J
			SNJ54S241J	SNJ54S241J
			SN54S244J	SN54S244J
			SNJ54S244J	SNJ54S244J
	CFP – W	Tube	SNJ54LS240W	SNJ54LS240W
			SNJ54LS241W	SNJ54LS241W
			SNJ54LS244W	SNJ54LS244W
			SNJ54S240W	SNJ54S240W
			SNJ54S241W	SNJ54S241W
			SNJ54S244W	SNJ54S244W
	LCCC – FK	Tube	SNJ54LS240FK	SNJ54LS240FK
			SNJ54LS241FK	SNJ54LS241FK
			SNJ54LS244FK	SNJ54LS244FK
			SNJ54S240FK	SNJ54S240FK
			SNJ54S241FK	SNJ54S241FK
			SNJ54S244FK	SNJ54S244FK

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

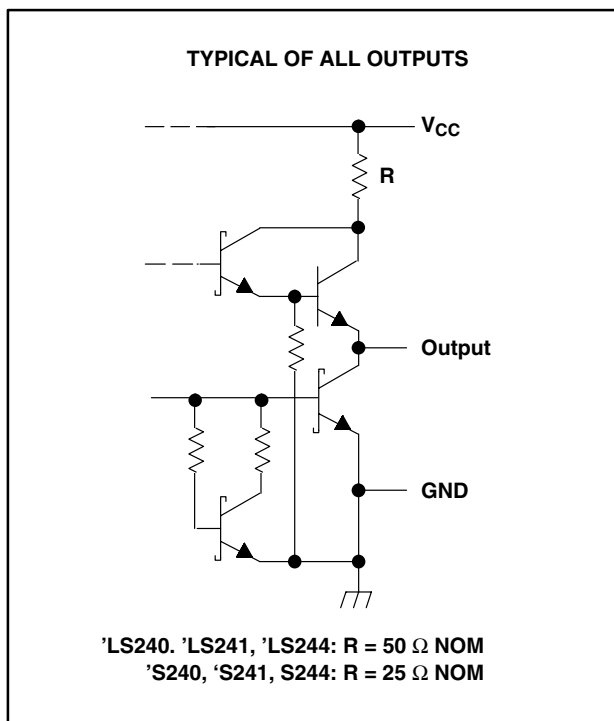
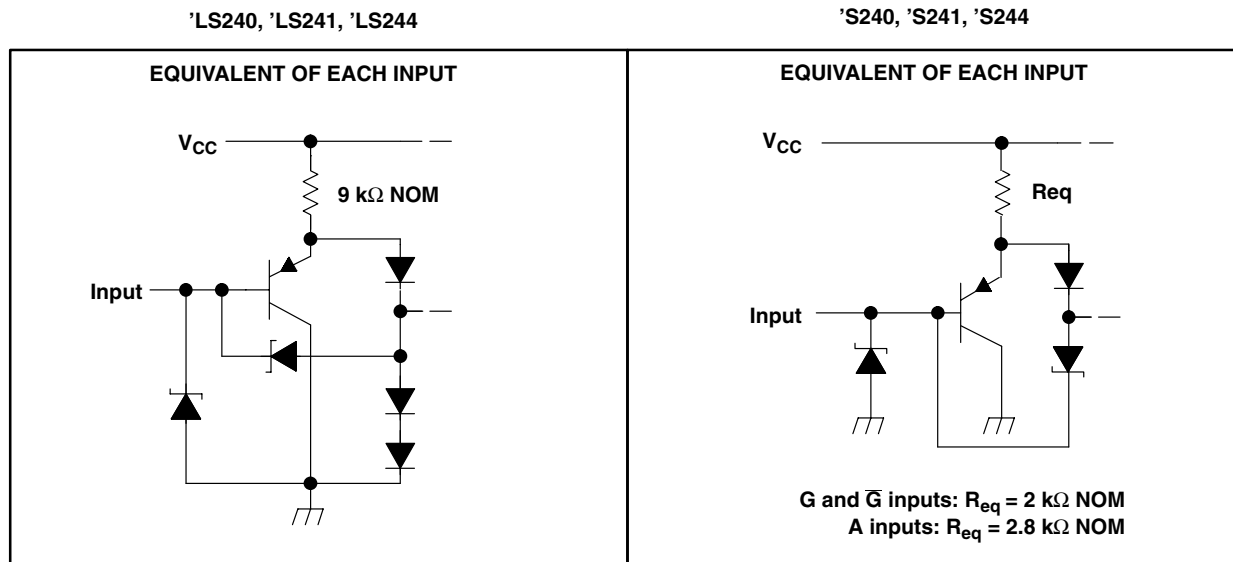
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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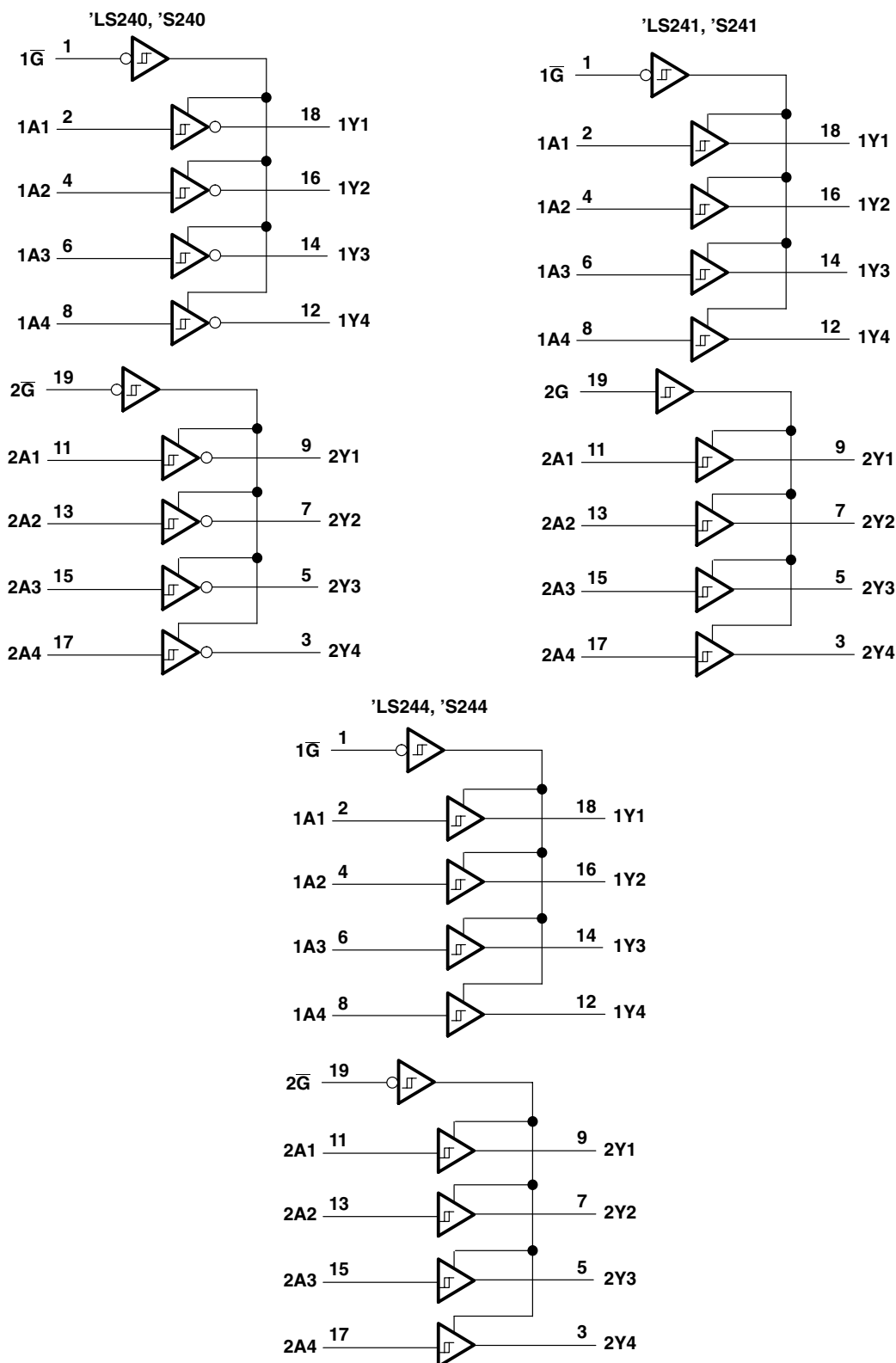
schematics of inputs and outputs



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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logic diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages.



SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : 'LS	7 V
'S	5.5 V
Off-state output voltage	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-12			-15	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS'		SN74LS'		UNIT	
			MIN	TYP‡	MAX	MIN		TYP‡
V_{IK}	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$			-1.5	-1.5	V	
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$		0.2	0.4	0.2	0.4	V	
V_{OH}	$V_{CC} = \text{MIN}$, $I_{OH} = -3 \text{ mA}$	$V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$,	2.4	3.4	2.4	3.4	V	
	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.5 \text{ V}$,	2		2			
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V}$,	$I_{OL} = 12 \text{ mA}$		0.4	0.4	V	
			$I_{OL} = 24 \text{ mA}$			0.5		
I_{OZH}	$V_{CC} = \text{MAX}$, $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V}$,			20	20	μA	
I_{OZL}	$V_{CC} = \text{MAX}$, $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V}$,			-20	-20	μA	
I_I	$V_{CC} = \text{MAX}$,	$V_I = 7 \text{ V}$			0.1	0.1	mA	
I_{IH}	$V_{CC} = \text{MAX}$,	$V_I = 2.7 \text{ V}$			20	20	μA	
I_{IL}	$V_{CC} = \text{MAX}$,	$V_{IL} = 0.4 \text{ V}$			-0.2	-0.2	mA	
$I_{OS}§$	$V_{CC} = \text{MAX}$,				-40	-225	mA	
I_{CC}	$V_{CC} = \text{MAX}$, Output open	Outputs high	All	17	27	17	27	mA
		Outputs low	'LS240	26	44	26	44	
			'LS241, 'LS244	27	46	27	46	
		Outputs disabled	'LS240	29	50	29	50	
'LS241, 'LS244	32		54	32	54			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	TEST CONDITIONS		'LS240		'LS241, 'LS244		UNIT
			MIN	TYP	MAX	MIN	
t_{PLH}	$R_L = 667 \Omega$,	$C_L = 45 \text{ pF}$	9	14	12	18	ns
t_{PHL}			12	18	12	18	
t_{PZL}	$R_L = 667 \Omega$,	$C_L = 45 \text{ pF}$	20	30	20	30	ns
t_{PZH}			15	23	15	23	
t_{PLZ}	$R_L = 667 \Omega$,	$C_L = 5 \text{ pF}$	10	20	10	20	ns
t_{PHZ}			15	25	15	25	



SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54S'			SN74S'			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V		
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage	0.8			0.8			V		
I_{OH}	High-level output current	-12			-15			mA		
I_{OL}	Low-level output current	48			64			mA		
	External resistance between any input and V_{CC} or ground	40			40			k Ω		
T_A	Operating free-air temperature (see Note 3)	-55			125			0	70	$^{\circ}$ C

NOTES: 1. Voltage values are with respect to network ground terminal.
3. An SN54S241J operating at free-air temperature above 116 $^{\circ}$ C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 40 $^{\circ}$ C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S'			SN74S'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$		-1.2			-1.2			V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$		0.2	0.4		0.2	0.4		V
V_{OH}	$V_{CC} = \text{MIN}$ $I_{OH} = -1 \text{ mA}$	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$,				2.7			V
	$V_{CC} = \text{MIN}$, $I_{OH} = -3 \text{ mA}$	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$,	2.4	3.4		2.4	3.4		
	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.5 \text{ V}$,	2			2			
V_{OL}	$V_{CC} = \text{MIN}$, $I_{OL} = \text{MAX}$	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$,	0.55			0.55			V
I_{OZH}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.8 \text{ V}$	$V_{IH} = 2 \text{ V}$, $V_O = 2.4 \text{ V}$	50			50			μ A
I_{OZL}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.8 \text{ V}$	$V_{IH} = 2 \text{ V}$, $V_O = 0.5 \text{ V}$	-50			-50			μ A
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		1			1			mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		50			50			μ A
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$	Any A	-400			-400			μ A
		Any G	-2			-2			mA
I_{OS}^{\S}	$V_{CC} = \text{MAX}$		-50	-225		-50	-225		mA
I_{CC}	$V_{CC} = \text{MAX}$, Output open	Outputs high	'S240	80	123	80	135	mA	
			'S241, 'S244	95	147	95	160		
		Outputs low	'S240	100	145	100	150		
			'S241, 'S244	120	170	120	180		
		Outputs disabled	'S240	100	145	100	150		
			'S241, 'S244	120	170	120	180		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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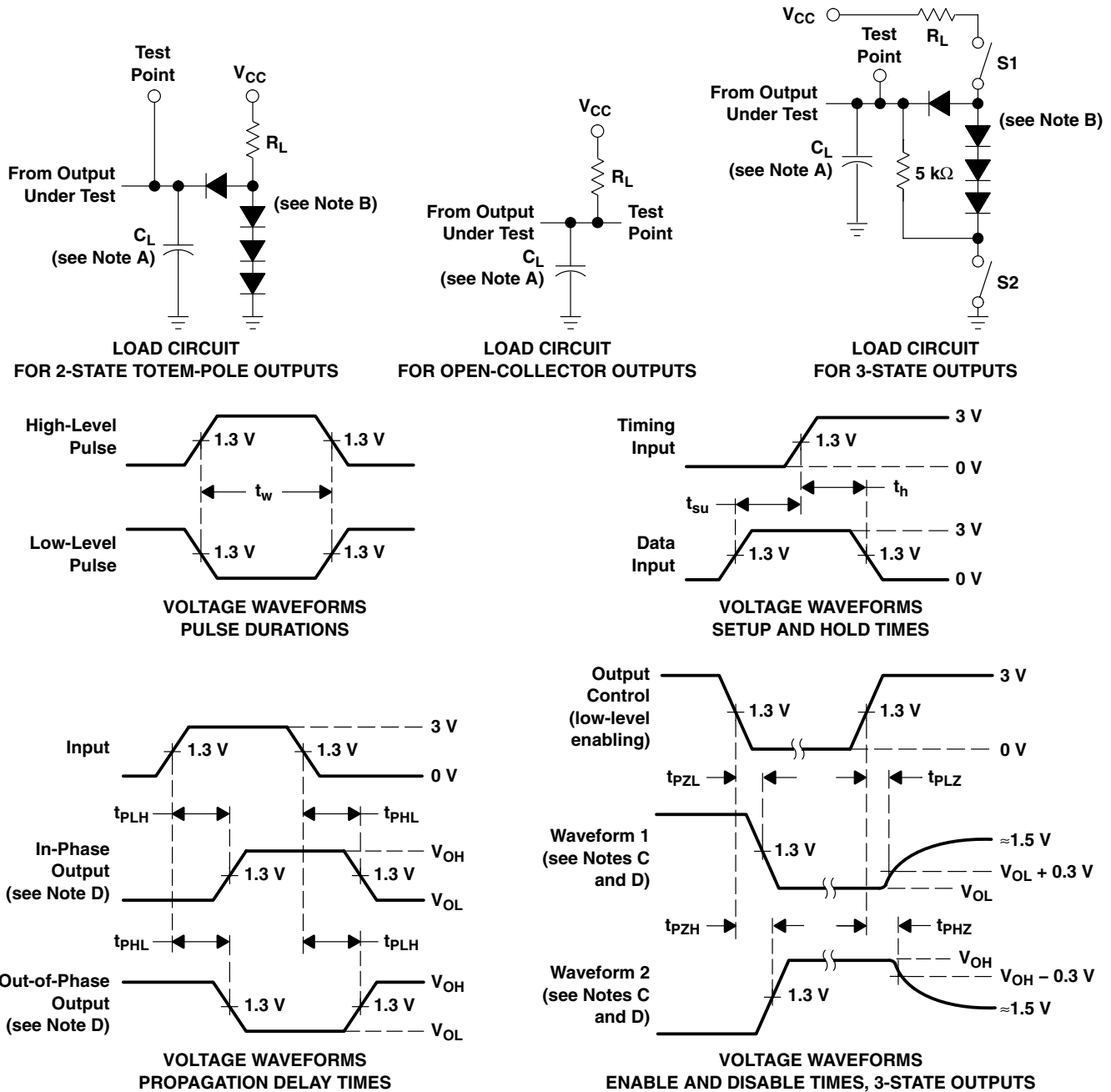
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER	TEST CONDITIONS	'S240			'S241, 'S244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 90\ \Omega$, $C_L = 50\ \text{pF}$	4.5	7		6	9	ns	
t_{PHL}		4.5	7		6	9		
t_{PZL}	$R_L = 90\ \Omega$, $C_L = 50\ \text{pF}$	10	15		10	15	ns	
t_{PZH}		6.5	10		8	12		
t_{PLZ}	$R_L = 90\ \Omega$, $C_L = 5\ \text{pF}$	10	15		10	15	ns	
t_{PHZ}		6	9		6	9		

**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES**



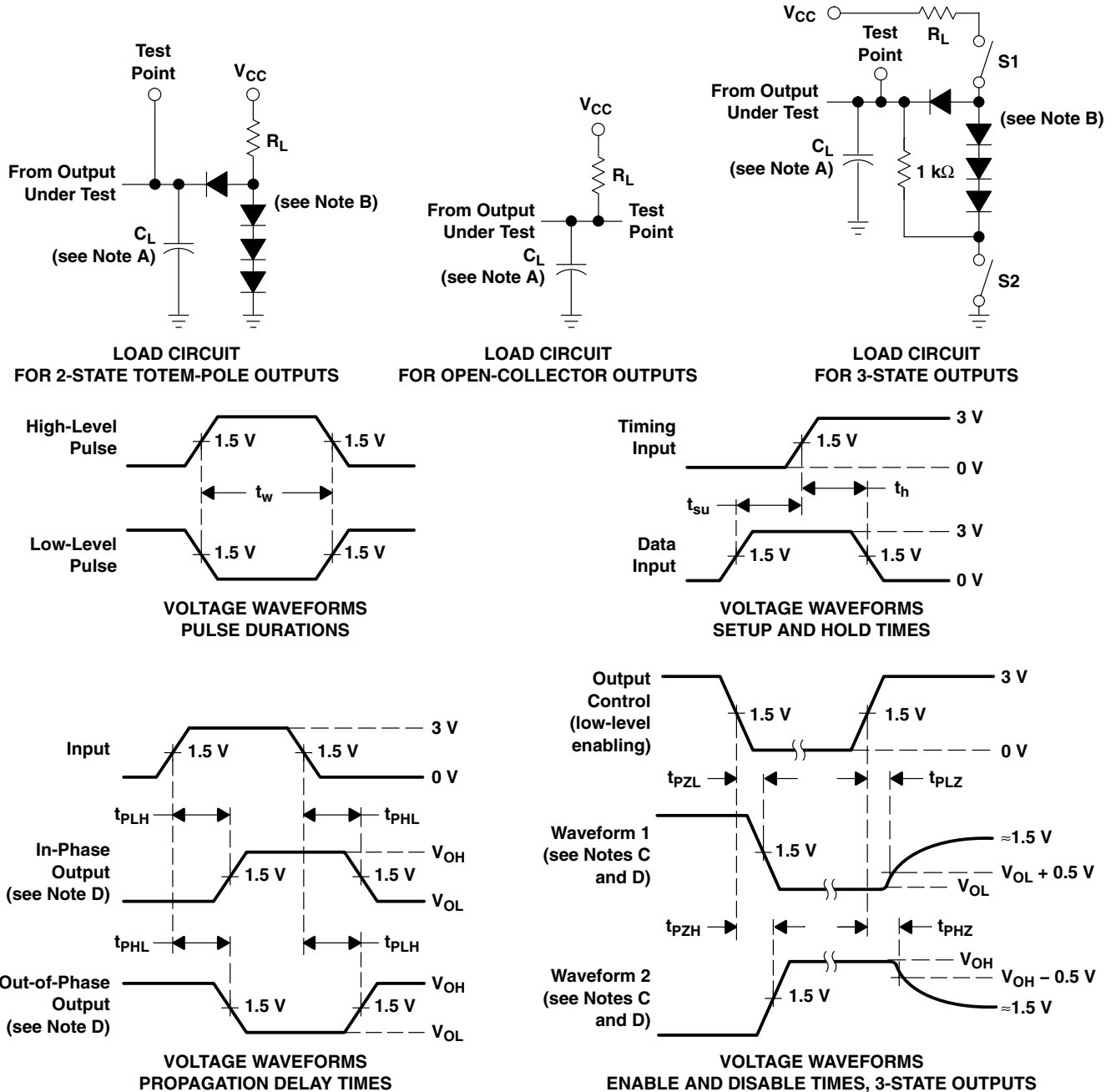
- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION
 SERIES 54S/74S DEVICES



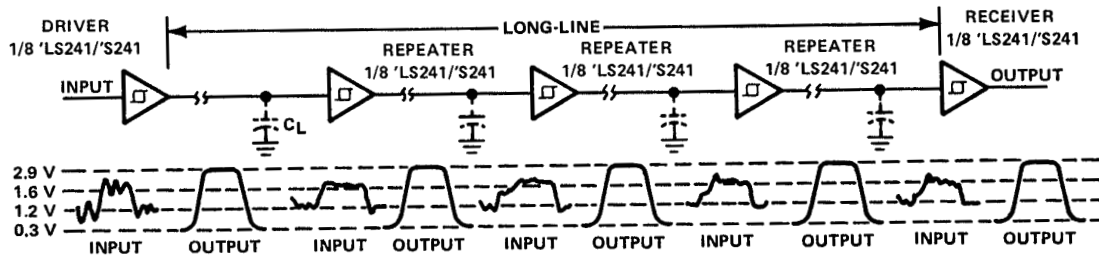
- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZL} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

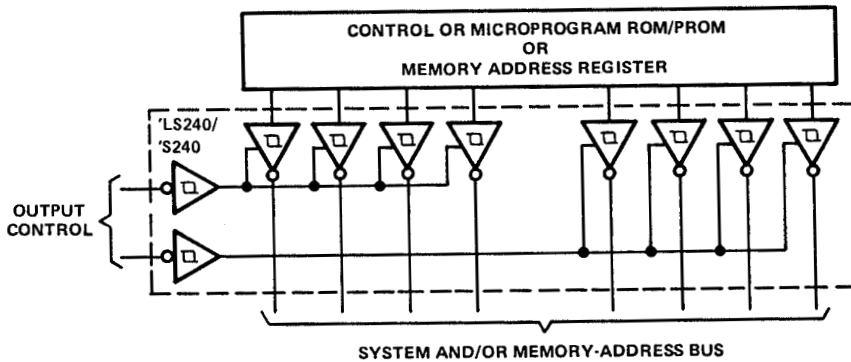
SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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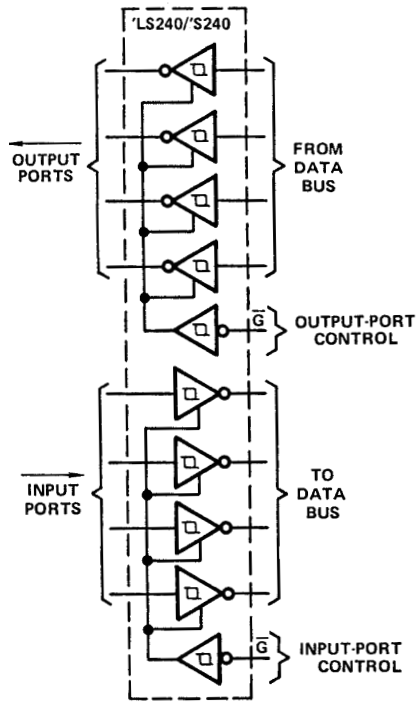
APPLICATION INFORMATION



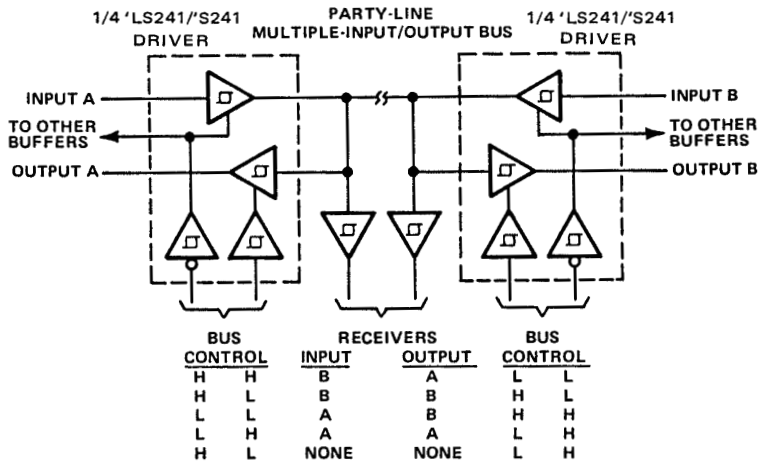
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS240NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74LS241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS241NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74LS244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS244NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74S240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74S241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74S244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS240DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS241DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS241NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS244DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74S240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74S241DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74S244DWR	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

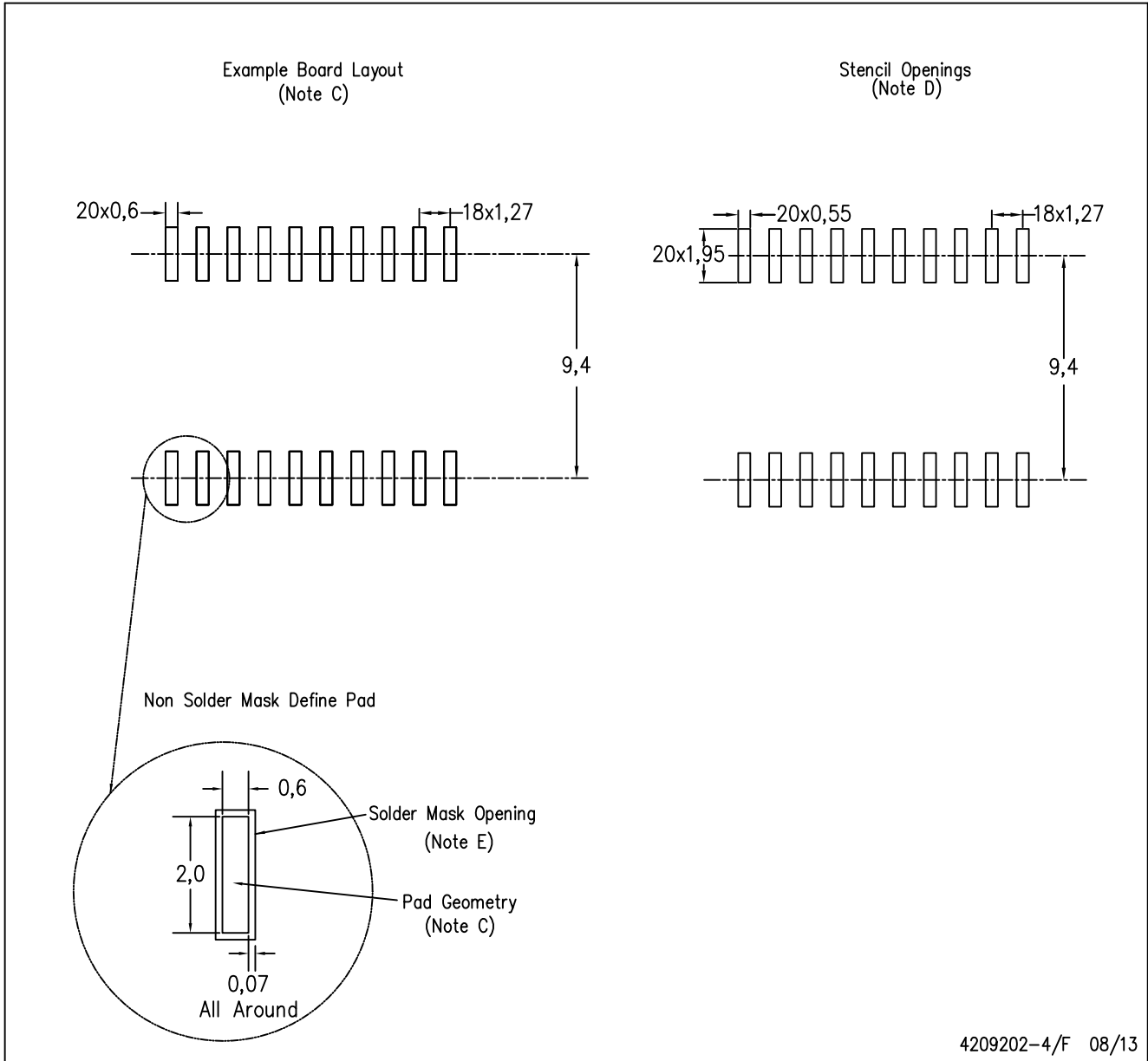
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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